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EXAMINER	
DICKEY, THOMAS L	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/529,433	TOUMIYA, YOSHINORI	
	Examiner	Art Unit	
	Thomas L. Dickey	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 April 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16,18 and 20-22* is/are pending in the application.

4a) Of the above claim(s) *1-11* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *12-16,18 and 20-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 March 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. The amendment filed on 04/02/2007 has been entered.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

Claims 16 and 20 stand rejected under 35 U.S.C. 102(a) as being anticipated by TANAKA (JP-2002110953).

Tanaka discloses a solid-state imaging device comprising a plurality of pixels arranged each including a light-receiving portion 102 and a MOS transistor 103, uppermost metallic Al layer wirings 106-107 positioned on both sides of said light-receiving portion 102 and asymmetrically disposed with respect to said light-receiving portion 102, and a single intra-layer lens formed without being affected by said asymmetrical uppermost wirings 106-107 and corresponding to each of said light-receiving portions 102. Note figure 1 and paragraphs 0020-0030 of Tanaka.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

A. Claims 12,13, and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over INOUE ET AL. (6,211,509) in view of Ogawa (6,104,021).

With regard to claims 12 and 13 Inoue et al. discloses a method for manufacturing a conventional (as of a date perhaps 4 years prior to Applicant's invention) solid-state imaging device comprising the steps of forming a plurality of light-receiving portions 42 on the surface of a substrate 41; forming wirings 47 on both sides of each of said light-receiving portions 42; wherein uppermost metallic layer wirings 47 are positioned on both sides of said light-receiving portion 42 and asymmetrically disposed with respect to said light-receiving portion 42, and a single intra-layer lens 49 formed without being affected by said asymmetrical uppermost wirings 47 and corresponding to each of said light-receiving portions 42; and prior to the step of forming said wirings 47, forming a charge readout transistor 23; forming a gate electrode 26 to operate said charge readout transistor 23; and forming a planarizing film 36 which covers said gate

electrode, wherein said wirings 47 and are formed above said planarizing film 36. Note figure 4, column 1, and column 2 lines 1-63 of Inoue et al. Inoue et al. provides a thorough grounding in the type of device Applicants now claim, but Inoue et al. does not disclose the steps of forming a first insulation layer having a first refractive index; etching said first insulation layer by using an etching mask and forming a concave portion above said planarizing film over each of said light–receiving portions; and forming a second insulation layer with a second refractive index to bury said concave portion.

However, Ogawa discloses a method for manufacturing a solid-state imaging device comprising the steps of forming a first insulation layer 38 having a first refractive index; etching said first insulation layer 38 by using an etching mask 40 and forming a concave portion 38a above a planarizing film 33c over each of a group of light-receiving portions 31; and forming a second insulation layer 32 with a second refractive index to bury said concave portion 38a. Note figures 3, 4, 5a-c, columns 5-7, and column 8 lines 1-38 of Ogawa. It would have been obvious to a person having skill in the art to modify Inoue et al.'s method by adding the steps of forming a first insulation layer having a first refractive index; etching said first insulation layer by using an etching mask and forming a concave portion above said planarizing film over each of said light–receiving portions; and forming a second insulation layer with a second refractive index to bury said

concave portion, as taught by as taught by Ogawa, thus achieving the claimed invention. The Examiner explicitly states that the reason (See *KSR International Co. v. Teleflex Inc.,* 550 U. S. __ (2007), slip op. at 14) for combining elements separately taught in Inoue et al. and Ogawa is that, as Ogawa explains at column 9 lines 39-54:

> When using the buried miniature lens 53, the designer easily optimizes the optical characteristics for the photo diode 31. Because there are various design factors independently changeable, i.e., the ratio of refractive index between the transparent material for the thick layer 38 and the transparent material for the convex lens 53d, the radius of curvature of the surface defining the generally semi-spherical recess 38c, the thickness of the transparent layer 38, the ratio of refractive index between the transparent material for the first transparent layer 53a and the transparent material for the convex lens 53d, the configuration of the curved upper surface 53c and the thickness of each transparent layer 38/53a/53d affect the optical characteristics of the solid state image sensing element 50, and the designer independently changes these factors.

With regard to claim 21 Inoue et al. discloses a method for manufacturing a conventional (as of a date perhaps 4 years prior to Applicant's invention) solid-state imaging device comprising the step of forming wirings 47 on a semi-conductor region 41 in which a plurality of pixels 42-43 each including a light-receiving portion 42 and a MOS transistor 43 are arranged through an insulation layer with the light-receiving portion 42 in between; wherein uppermost metallic layer wirings 47 are positioned on both sides of said light-receiving portion 42 and asymmetrically disposed with respect to said light-receiving portion 42, and a single intra-layer lens 49 formed without being affected by said asymmetrical uppermost wirings 47 and corresponding to each of said light-receiving portions 42. Note figure 4, column 1, and column 2 lines 1-63 of Inoue et al. Inoue et al. provides a thorough grounding in the type of device Applicants now claim,

but Inoue et al. does not disclose the steps of forming a first insulation layer with a first refractive index across the whole surface thereof; selectively removing said first insulation layer with a etching mask by isotropic-etching at a position corresponding to said light-receiving portion to form a concave portion corresponding to each light-receiving portion; forming a second insulation layer with a second refractive index across the whole surface including said concave portion; and planarizing said second insulation layer and making the second insulation layer remain within said concave portion to form the single intra-layer lens from said first and second insulation layers.

However, Ogawa discloses a method for manufacturing a solid-state imaging device comprising the steps of forming a first insulation layer 38 with a first refractive index across the whole surface thereof; selectively removing said first insulation layer 38 with a etching mask 40 by isotropic-etching at a position corresponding to a light-receiving portion to form a concave portion 38a corresponding to each light-receiving portion; forming a second insulation layer 32 with a second refractive index across the whole surface including said concave portion 38a; and planarizing said second insulation layer 32 and making the second insulation layer 32 remain within said concave portion 38a to form a single intra-layer lens 53 comprising said first 38 and second 32 insulation layers. Note figures 3, 4, 5a-c, columns 5-7, and column 8 lines 1-38 of Ogawa. It would have been obvious to a person having skill in the art to modify Inoue et al.'s method by

adding the steps of forming a first insulation layer with a first refractive index across the whole surface thereof; selectively removing said first insulation layer with a etching mask by isotropic-etching at a position corresponding to said light-receiving portion to form a concave portion corresponding to each light-receiving portion; forming a second insulation layer with a second refractive index across the whole surface including said concave portion; and planarizing said second insulation layer and making the second insulation layer remain within said concave portion to form the single intra-layer lens from said first and second insulation layers, as taught by Ogawa, thus achieving the claimed invention. The Examiner explicitly states that the reason (See *KSR International Co. v. Teleflex Inc.*, 550 U. S. __ (2007), slip op. at 14) for combining elements separately taught in Inoue et al. and Ogawa is that, as Ogawa explains at column 9 lines 39-54:

> When using the buried miniature lens 53, the designer easily optimizes the optical characteristics for the photo diode 31. Because there are various design factors independently changeable, i.e., the ratio of refractive index between the transparent material for the thick layer 38 and the transparent material for the convex lens 53d, the radius of curvature of the surface defining the generally semi-spherical recess 38c, the thickness of the transparent layer 38, the ratio of refractive index between the transparent material for the first transparent layer 53a and the transparent material for the convex lens 53d, the configuration of the curved upper surface 53c and the thickness of each transparent layer 38/53a/53d affect the optical characteristics of the solid state image sensing element 50, and the designer independently changes these factors.

B. Claims 14, 15, and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over INOUE ET AL. (6,211,509) in view of Ogawa (6,104,021) and MATSUDA ET AL. (JP11-40787).

With regard to claims 14 and 15 Inoue et al. discloses a method for manufacturing a solid-state imaging device comprising the steps of forming a plurality of light-receiving portions 42 on the surface of a substrate 41; forming wirings 47 on both sides of each of said light-receiving portions 42; wherein uppermost metallic layer wirings 47 are positioned on both sides of said light-receiving portion 42 and asymmetrically disposed with respect to said light-receiving portion 42, and a single intra-layer lens 49 formed without being affected by said asymmetrical uppermost wirings 47 and corresponding to each of said light-receiving portions 42. Note figure 4, column 1, and column 2 lines 1-63 of Inoue et al. Inoue et al. provides a thorough grounding in the type of device Applicants now claim, but Inoue et al. does not disclose the steps of forming a first insulation layer with a first refractive index; forming a second insulation layer with a second refractive index on said first insulation layer; and forming a third insulation layer to cover said convex surface of said first insulation layer prior to the step of forming said second insulation layer, or the steps of forming a reflow film with a convexly curved surface at a position corresponding to the respective light-receiving portions and etching back said reflow film with the first insulation layer to transfer said convexly curved surface onto the first insulation layer.

However, Ogawa discloses a method for manufacturing a solid-state imaging device comprising the steps of forming a first insulation layer 38 with a first refractive index;

forming a second insulation layer 53d with a second refractive index on said first insulation layer 38; and forming a third insulation layer 53a to cover said convex surface of said first insulation layer 38 prior to the step of forming said second insulation layer 53d. Note figure 6, column 8 lines 39-67, and column 9 lines 1-38 of Ogawa. Further, Matsuda et al. discloses a method for manufacturing a solid-state imaging device comprising, inter alia, the steps of forming a reflow film 7 with a convexly curved surface at a position corresponding to light-receiving portions and etching back said reflow film 7 with a first insulation layer 6 to transfer said convexly curved surface onto the first insulation layer 6. Note figure 2 and paragraphs 0016-0020 of Matsuda et al. It would further have been obvious to a person having skill in the art to augment Ogawa's method with the steps of forming a reflow film with a convexly curved surface at a position corresponding to light-receiving portions and etching back said reflow film with a first insulation layer to transfer said convexly curved surface onto the first insulation layer, such as taught by Matsuda et al. The Examiner explicitly states (See *KSR International Co. v. Teleflex Inc.,* 550 U. S. __ (2007), slip op. at 14) that there are two reason for combining elements separately taught in Inoue et al., Ogawa, and Matsuda et al. In the first instance, as Ogawa explains at column 9 lines 39-54:

> When using the buried miniature lens 53, the designer easily optimizes the optical characteristics for the photo diode 31. Because there are various design factors independently changeable, i.e., the ratio of refractive index between the transparent material for the thick layer 38 and the transparent material for the convex lens 53d, the radius of curvature of the surface defining the generally semi-spherical recess 38c, the thickness of the transparent layer 38, the ratio of refractive index between the

> transparent material for the first transparent layer 53a and the transparent material for the convex lens 53d, the configuration of the curved upper surface 53c and the thickness of each transparent layer 38/53a/53d affect the optical characteristics of the solid state image sensing element 50, and the designer independently changes these factors.

Secondly, it would have made sense to one of skill in the art to augment Ogawa's method with the steps of forming a reflow film with a convexly curved surface at a position corresponding to light-receiving portions and etching back said reflow film with a first insulation layer to transfer said convexly curved surface onto the first insulation layer, such as taught by Matsuda et al. in order to form the interlayer lens in a desired shape with improved condensing efficiency.

With regard to claim 22 Inoue et al. discloses a method for manufacturing a solid-state imaging device comprising the steps of forming wirings 47 on a semi-conductor region 41 in which a plurality of pixels 42-43-44-45 each including a light-receiving portion 42 and a MOS transistor 43 are arranged through an insulation layer 96 with the light-receiving portion 42 in between; wherein uppermost metallic layer wirings 47 are positioned on both sides of said light-receiving portion 42 and asymmetrically disposed with respect to said light-receiving portion 42, and a single intra-layer lens 49 formed without being affected by said asymmetrical uppermost wirings 47 and corresponding to each of said light-receiving portions 42. Note figure 4, column 1, and column 2 lines 1-63 of Inoue et al. Inoue et al. provides a thorough grounding in the type of device Applicants now claim, but Inoue et al. does not disclose the steps of forming a first

insulation layer with a first refractive index across the whole surface thereof; and forming a planarizing film with a second refractive index on said first insulation layer to form said single intra-layer lens including said first insulation layer and said planarizing film, or the steps of forming a reflow film with a convexly curved surface at a position corresponding to the respective light-receiving portions and etching back said reflow film with the first insulation layer to transfer said convexly curved surface onto the first insulation layer.

However, Ogawa discloses a method for manufacturing a solid-state imaging device comprising the steps of forming a first insulation layer 38 with a first refractive index across the whole surface thereof; and forming a planarizing film 53d with a second refractive index on said first insulation layer 38 to form a single intra-layer lens 53 including said first insulation layer 38 and said planarizing film 53d. Note figure 6, column 8 lines 39-67, and column 9 lines 1-38 of Ogawa. Further, Matsuda et al. discloses a method for manufacturing a solid-state imaging device comprising, inter alia, the steps of forming a reflow film 7 with a convexly curved surface at a position corresponding to light-receiving portions and etching back said reflow film 7 with a first insulation layer 6 to transfer said convexly curved surface onto the first insulation layer 6. Note figure 2 and paragraphs 0016-0020 of Matsuda et al. It would further have been obvious to a person having skill in the art to augment Ogawa's method with the steps of

forming a reflow film with a convexly curved surface at a position corresponding to light-receiving portions and etching back said reflow film with a first insulation layer to transfer said convexly curved surface onto the first insulation layer, such as taught by Matsuda et al. The Examiner explicitly states (See *KSR International Co. v. Teleflex Inc.*, 550 U. S. __ (2007), slip op. at 14) that there are two reason for combining elements separately taught in Inoue et al., Ogawa, and Matsuda et al. In the first instance, as Ogawa explains at column 9 lines 39-54:

> When using the buried miniature lens 53, the designer easily optimizes the optical characteristics for the photo diode 31. Because there are various design factors independently changeable, i.e., the ratio of refractive index between the transparent material for the thick layer 38 and the transparent material for the convex lens 53d, the radius of curvature of the surface defining the generally semi-spherical recess 38c, the thickness of the transparent layer 38, the ratio of refractive index between the transparent material for the first transparent layer 53a and the transparent material for the convex lens 53d, the configuration of the curved upper surface 53c and the thickness of each transparent layer 38/53a/53d affect the optical characteristics of the solid state image sensing element 50, and the designer independently changes these factors.

Secondly, it would have made sense to one of skill in the art to augment Ogawa's method with the steps of forming a reflow film with a convexly curved surface at a position corresponding to light-receiving portions and etching back said reflow film with a first insulation layer to transfer said convexly curved surface onto the first insulation layer, such as taught by Matsuda et al. in order to form the interlayer lens in a desired shape with improved condensing efficiency.

C. Claim 18 stands rejected under 35 U.S.C. 103(a) as being unpatentable over TANAKA (JP-2002110953) in view of YAMAGUCHI ET AL. (6,344,666).

Tanaka discloses a solid-state imaging device comprising a plurality of pixels including all the limitations of claim 18 except the limitation that the center of said intra-layer lens is biased to the center side of an imaging region from the center of said light-receiving portion, when approaching the periphery of the imaging region. Note figure 1 and paragraphs 0020-0030 of Tanaka.

However, Yamaguchi et al. discloses a solid-state imaging device comprising a plurality of pixels including an intra-layer lens 27 whose center is biased to the center side of an imaging region (the imaging region spans the entire imaging device from the center of a light-receiving portion 21, when approaching the periphery of the imaging region. Note figure 2 and column 2 lines 32-39 of Yamaguchi et al. Therefore, it would have been obvious to a person having skill in the art to modify Tanaka's solid-state imaging device by biasing the center of the intra-layer lens to the center side of the imaging region from the center of the light-receiving portion, when approaching the periphery of the imaging region, such as taught by Yamaguchi et al. in order to properly adjust the relative sensitivities of the peripheral and central light-receiving portions, as Yamaguchi et al. explains in column 1 lines 48-67.

Response to Arguments

4. Applicant's arguments with respect to claims 12-15 and 22 have been considered but are moot in view of the new ground(s) of rejection.

5. With regard to claim 16 (formerly 19), 18, and 20, Applicant's arguments filed 04/02/2007 have been fully considered but they are not persuasive.

It is argued, at page 7 of the remarks, that (in Applicant's figure 3) "Part of uppermost layer wirings 7 and 8 positioned on both sides of the light-receiving portion 2 are asymmetrically disposed with respect to the light-receiving portion 2 (in the illustrative example, wiring 8 is closer to the light-receiving portion 2 than wiring 8 [typo for "wiring 7?" there is only one wiring 8 per light-receiving portion)." However, the asymmetrically disposed wirings of claim 16 are required, by the claim, to be "positioned on both sides of at least one of said light-receiving portions." Note line 5 of claim 16. In figure 3, wiring 8 is formed on only one side of the light-receiving portion. Therefore, wiring 8 cannot represent the "uppermost layer wirings positioned on both sides of said light-receiving portion" of claim 16. Only wirings 7, which are positioned on both sides, can represent the claimed wirings. Did Applicant mean, when he wrote, "uppermost layer wirings positioned on both sides of said light-receiving portion [that] are asymmetrically disposed with respect to said light-receiving portion," to claim

symmetrically disposed wirings (like wirings 7) positioned on both sides of the light-receiving portion, and in addition, asymmetric wirings (like wirings 8) that are not positioned on both sides of the light-receiving portion? That's not precisely the wording of claim 16.

Applicant argues, at page 8 of the remarks, that "Tanaka's wirings 106 and 107 are symmetrically positioned and at an equal distance from each side of light-receiving portion 102. Unlike Applicant's claimed invention, nowhere does Tanaka disclose or suggest wirings positioned on both sides of a light-receiving portion that are asymmetrically disposed with respect to the light-receiving portion." However, Tanaka's wirings 106 and 107 are equally as asymmetric as the "uppermost layer wirings 7" of Applicant's figure 3. As explained above, the claimed "asymmetrically disposed" wirings must necessarily be represented by Applicant's wirings 7, as these are the only wirings Applicant discloses as "positioned on both sides of a light-receiving portion," as required by the claim.

6. Applicant claims priority, for the various claims of this application, from either Japanese Patent Application P2003-284352 or P2003-070750. It is noted that both P2003-284352 and P2003-070750 have been pending at the JPO for in excess of four years. Has Applicant received any relevant communication from JPO concerning these

applications? Or has Applicant, perhaps, abandoned these cases at the JPO in favor of his international filings based on PCT/JP03/11915?

Conclusion

7. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thomas L. Dickey whose telephone number is 571-272-1913. The examiner can normally be reached on Monday-Thursday 8-6.

If attempts to reach the examiner by telephone are unsuccessful, please contact the examiner's supervisor, Sue A. Purvis, at 571-272-1236. The fax phone number for the

organization where this application or proceeding is assigned is 571-273-8300. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Thomas L. Dickey/
Primary Examiner
Art Unit 2826